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Attorney Docket No. 2207/10615
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

INVENTOR: Zhong-Ning (George) CAI

SERIAL NO: 09/749,792

FILING DATE: December 28, 2000

TITLE: METHOD AND APPARATUS FOR THERMAL SENSITIVITY BASED ON DYNAMIC POWER CONTROL

ART UNIT: 2116

EXAMINER: Tse W. CHEN

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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Dated: January 29, 2006

Pilar Rodriguez

ATTENTION: Board of Patent Appeals and Interferences

REQUEST FOR RECONSIDERATION

SIR:

Appellant respectfully requests reconsideration of the decision of the Board of Patent Appeals and Interferences that was mailed on November 29, 2006. Among other things, the Board's decision affirmed the rejection of claims 1-20 under 35 U.S.C. §103. Appellant submits that in affirming these rejections the Board's decision misapprehended Appellant's arguments and that, for these reasons, this decision should be reheard and the rejections of claims 1 through 20 should be reversed. In particular, Appellant respectfully submits that the Board overlooked or misapprehended Appellant's arguments that the prior art does not teach or suggest at least a "performance demanding level input" as described in claimed embodiments of the present application.

1. Background

Embodiments of the present invention relate to a frequency reduction circuit that includes a performance demanding level ("PDL") input to determine a rate of temperature-related frequency reduction. *See* e.g., independent claims 1, 7, 12, 18. Among other things, the PDL signal lets the frequency reduction circuit be sensitive to particular applications (i.e., the current "performance demand" of the system). For example, during a period of frequency reduction in response to high temperatures, if a hardware component (e.g. a hard drive) is running an application that does not require great processor speed, aggressive frequency reduction may be performed, by not asserting the PDL signal. On the other hand, if a hardware component requires high processor speed, frequency reduction with finer granularity may be performed by asserting the PDL signal.

During appeal, Applicant argued the cited references Georgiou et al. and McDermott do not suggest at least a performance demanding level input to determine a rate of temperature-related frequency reduction, as recited in each of independent claims 1, 7 and 12. Applicant further argued Georgiou and McDermott suggest nothing resembling the claimed PDL input feature. *See* Appeal Brief dated 10/24/2005, page 6. The Examiner recognized this with respect to Georgiou. *See* Final Office Action mailed 3/21/05, page 3, paragraph 6. However, the Examiner alleged that McDermott remedied this deficiency in Georgiou. *See* id.

In its decision, the Board held the Examiner's reliance on McDermott was cumulative since Georgiou teaches a performance demanding level input for determining

the rate of reduction of the temperature-related frequency. *See* Decision on Appeal, dated November 29, 2006, pages 11-12.

Applicant respectfully disagrees, requests reconsideration, and submits the following comments for consideration.

2. The Board overlooked or misapprehended Appellant's arguments that Georgiou fails to teach or suggest at least a "performance demanding level input"

The claims on appeal relate to thermal throttling in a processor. As stated above, the claimed "performance demanding level input" lets the frequency reduction circuit be sensitive to particular applications (i.e., the current "performance demand" of the system). Applicants submits the claimed PDL input, therefore, controls a rate of processor clock frequency reduction in accordance with *demand for performance*.

The "performance demanding level input" as described in embodiments of the present application is discussed throughout the specification. For example, paragraph [0020] (as cited and discussed in the Decision on Appeal, page 8) states:

> The performance demanding level signal (PDL) 311 is an input signal used by the frequency reduction circuit 305 to determine the level of sensitivity (or aggression) used for frequency reduction. *If PDL signal 311 is asserted (e.g., value of "1"), then frequency reduction cannot be aggressive and instead fine granularity must be used (e.g., 1/15 reduction from normal clock frequency) for reducing the normal clock frequency. Alternatively, if PDL signal 311 is not asserted (e.g., value of "0"), then frequency reduction can be aggressive and higher percentages of frequency reduction (e.g., close to 50% reduction from normal clock frequency) may be used for reducing the normal clock frequency.* Advantageously, the PDL signal 311 can be used as a form of hardware performance profiling for system components interconnected to processor architecture 300. (*emphasis added*)

Applicant submits the remaining portion of paragraph [0020] – not discussed in the Decision on Appeal – provides more clarification regarding the operation of the PDL signal.

> In an exemplary scenario, *during a period of frequency reduction in response to high temperatures, if a hardware component running an application (e.g., hard drive) does not require as close to possible full processor speed* (e.g., 1 Gigahertz - GHz), then aggressive frequency reduction may be performed (e.g., close to 50% reduction, 550 MHz) and the PDL signal 311 is not asserted. Alternatively, *if the hardware component does require as close to possible full processor speed for running its application during the high temperature period, then fine granularity of frequency reduction* (e.g., 5% reduction, 950 MHz) must be performed and the PDL signal 311 is asserted. (*emphasis added*)

In light of at least the sections discussed above, Applicant respectfully submits the plain meaning of this language is not ambiguous: a "performance demanding level input" in a processor, by its terms, describes an input that relates to a level of performance of the processor in accordance with demand.

Moreover, the PDL as described in embodiments of the present application is not directed toward simply reducing the clock frequency of the processor upon the meeting of a temperature threshold. Instead, it is directed toward determining *whether* an application requires close to possible full processor speed or not (i.e., "performance *demand* level"). If the processor approaches a temperature limit but nevertheless high performance is demanded, the performance demanding level input may assert a value that causes the frequency reduction to be less aggressive. If, on the other hand, the processor approaches a temperature limit but high performance is not demanded, the performance demanding level input may assert a value that causes the frequency reduction to be more aggressive. The performance demanding level input is dependent on and directly related to "performance demand".

Applicant submits the relevant sections of the cited reference Georgiou, on the other hand, are not directed toward monitoring or maintaining "performance" or assessing performance *requirements* of the system, but rather simply determining whether temperature of the processor has exceeded a predetermined threshold, and reducing clock frequency based upon such a comparison. In fact, upon discussing column 4, lines 26-50 and column 8, lines 55-66 of Georgiou, the Board itself concluded:

> Particularly, Georgiou teaches a thermal sensor and a comparator for determining *when the temperature of the processor has exceeded a predetermined threshold (i.e., overheating).* Further, Georgiou discloses that upon receipt of a signal (270) from the comparator indicating that the processor is overheating, the voltage regulators (330) reduce the supply voltage, and the clock selector (430) selects a modulated clock frequency (425) that correspondingly reduces the clock frequency down to a rate that can reduce the amount of power dissipated in the processor. (*emphasis* added) See Decision on Appeal dated November 29, 2006, pages 10-11.

Applicant submits the thermal sensor-processor embodiment taught in Georgiou is performance-dependent at all; it is temperature-dependent. As described in the Board's summary above, a temperature comparator is used to determine overheating, upon which the clock frequency of the processor is reduced. This determination is based on temperature and temperature alone; the "performance" or the "performance demand" of the system is not considered at all.

Therefore, Applicant submits the signal 270 of Georgiou from the temperature-dependent comparator indicating the processor is overheating does not teach or suggest a "*performance demanding* level input" as described in embodiments of the present application.

Applicants further submit McDermott fails to make up for the deficiencies of Georgiou for at least the reasons described in the Appeal Brief.

In order to support a proper rejection, the cited references must teach or suggest each and every limitation of the claim. As shown above and discussed in the Appeal Brief, the Georgiou, Ko and McDermott references fail to teach or suggest at least a "performance demanding level input" as described in claim 1. Independent claims 7, 12 and 18 contain similar allowable limitations. Claims 2-6, 8-11, 13-17 and 19-20 are likewise allowable over Georgiou, Ko and McDermott for at least the reason that they include the recitations of one of claims 1, 7, 12 and 18 by dependence thereon.

For at least these reasons, Appellant respectfully submits that the Board's decision of November 29, 2006, should be reheard and the rejections of claims 1 through 20 should be reversed.

Respectfully submitted,
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Dated: January 29, 2007

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Docket Number:	2207/10615	Total number of pages: (including cover)	7

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Application No.	:	09/749,792 Confirmation No. 6261
Applicant	:	Zhong-Ning (George) Cai
Filed	:	December 28, 2000
Title	:	METHOD AND APPARATUS FOR THERMAL SENSITIVITY BASED ON DYNAMIC POWER CONTROL
TC/A.U.	:	2116
Examiner	:	Tse W. Chen

PAPER(s) ENTITLED: Request for Reconsideration 6 pages

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